High-Performance Self-Capacitive Touch Chip V1.3

1. Overview

CST816D self-capacitance touch chip, using high-speed MCU core and embedded DSP circuit, combined with its own fast self-capacitance sensing technology, can widely support a variety of self-capacitance patterns including triangles. It can realize single-point gestures and real two-point operation, achieves extremely high sensitivity and low standby power consumption.

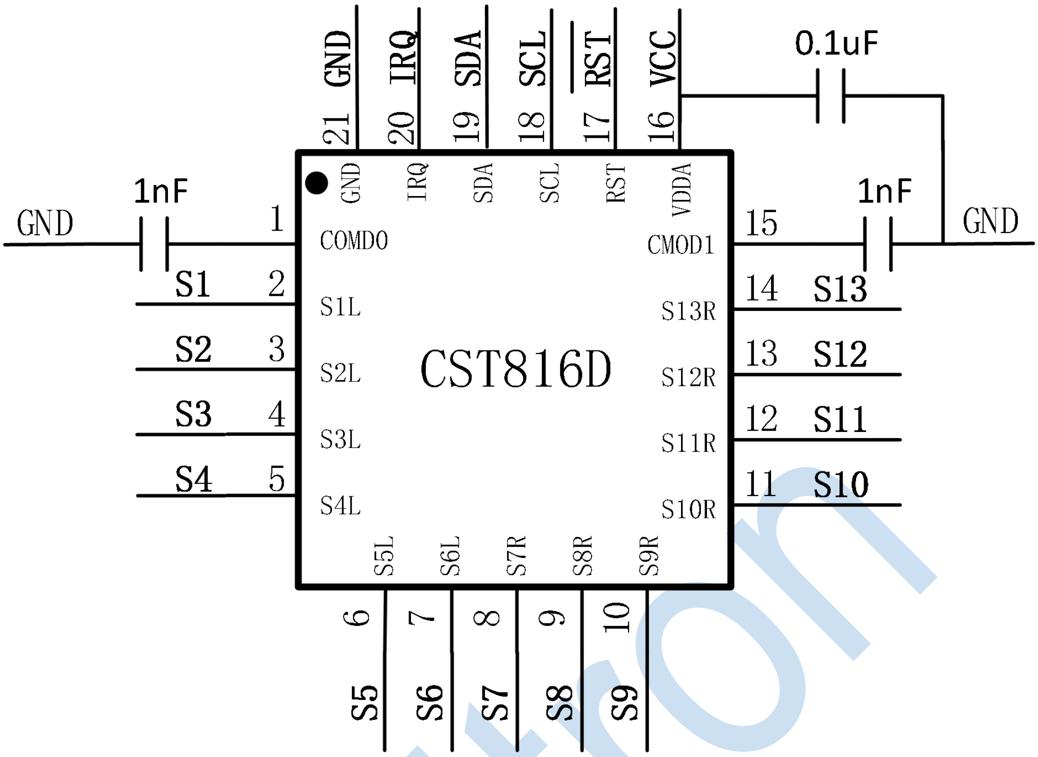
2. Chip Features

- **Built-in fast self-capacitance detection circuit and high-performance DSP module**
  - ✧ Supports online programming
  - ✧ Built-in watchdog
  - ✧ Supports multiple keys
  - ✧ Supports sleep gesture wake-up function
- **Capacitive Screen Support**
  - ✧ Supports up to 13 sensing channels
  - ✧ Supports channel floating/drop-down design
  - ✧ Automatic adjustment of module parameters
- **Performance Index**
  - ✧ Report rate > 100Hz
  - ✧ Single-point and two-point gesture operation
- **Power Consumption**
  - ✧ Typical power consumption in dynamic mode is 1.8mA.
  - ✧ Typical power consumption in sleep mode is 2uA.
- **Communication Interface**
  - ✧ I2C master/slave communication interface, the rate is 10Khz~400Khz configurable.
  - ✧ Compatible with 1.8V/3.3V interface level.
- **Power Supply**
  - ✧ Single power supply 2.8V ~ 3.6V, power supply ripple <= 50mv
- **Package Type**
  - ✧ QFN3X3-20L

3. Typical Applications

Consumer electronics, watches and other products

4. Reference Circuit



Reference Circuit Diagram

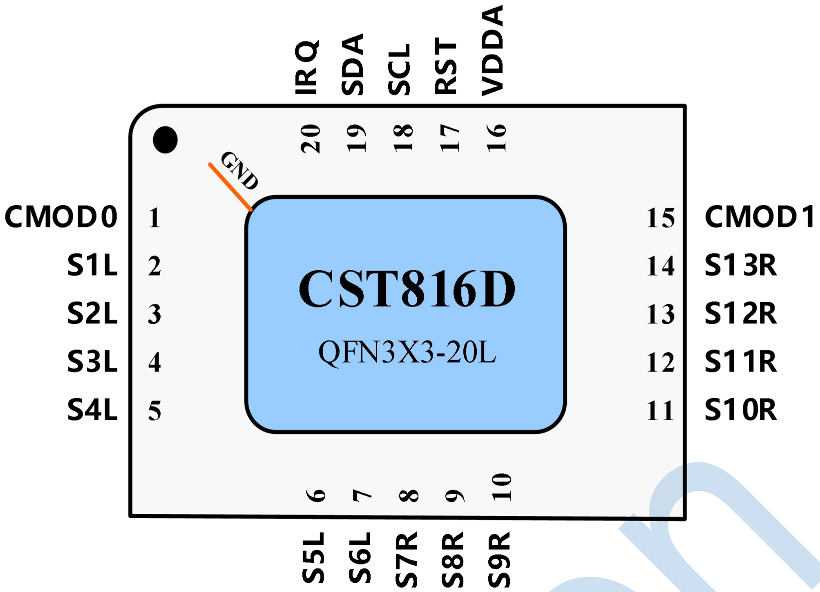
Precautions:

- ✓ Use NPO/COG material capacitors with at least 10% accuracy for CMOD filter capacitors.
- ✓ The selection range of CMOD capacitance value is between 1nF and 5.6nF, generally 1nF is selected. The specific optimum value is related to the corresponding body capacitance.
- ✓ The CMOD filter capacitor must be placed close to the corresponding pin of the chip, and the trace between CMOD and the chip should be as short as possible.

5. Ordering Information

Part No	Package	Marking	Packing	Description
CST816D	QFN3X3-20L	● CST816D XXXXX	take-up package (5000)	Dot: Pin1 Mark point CST816D: Model character XXXXX: 5-digit production tracking code

6. Pinout/Description



Pin Name	Description	Remark
S01~S13	Sensors	
VDDA	Power supply	2.8V~3.6V, connect to 2.2uF~ 10uF capacitor.
CMOD0/CMOD1	Voltage regulator capacitor	Connect to 1nF~5.6nF voltage regulator capacitor.
IRQ	Interrupt output	Rising/Falling edge selectable.
SCL/SDA	I2C	Optional internal pull-up/open-drain mode.
RST	Reset input	Low effective.
GND	Substrate	The substrate is GND and it must be connected.

Pin Description Table

Remark:

1. CMOD0/CMOD1 must be connected to a voltage regulator capacitor between 1nF ~ 5.6nF;

7. Function Description

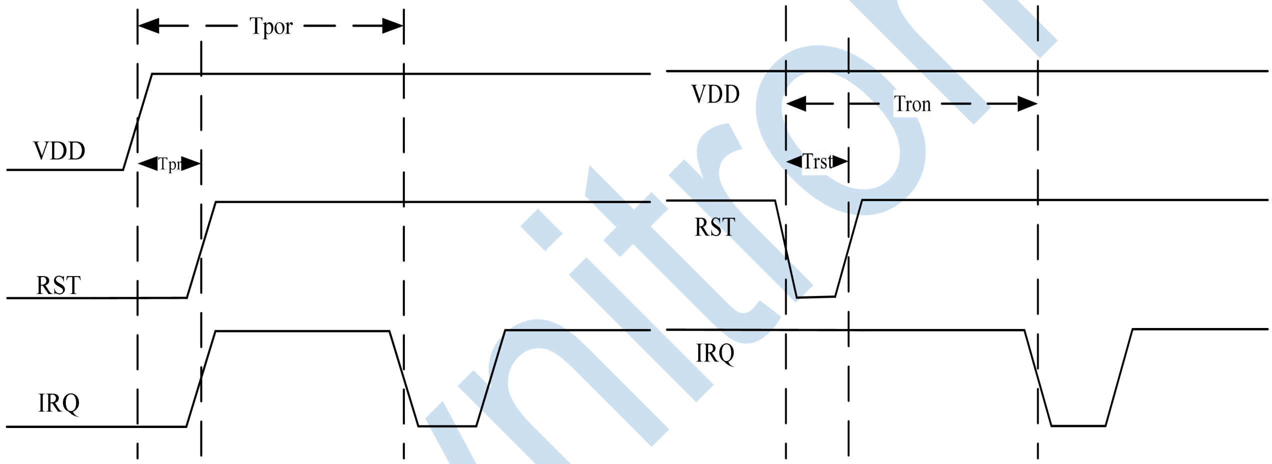
CST816D self-capacitance touch chip, with its built-in fast self-capacitance sensing module, it can realize single-point gestures and real two-point functions on patterns such as triangles without any external devices (except circuit bypass capacitors). Aside from its fast response, it has extremely excellent anti-noise, waterproof and low power consumption performance.

7.1. Power on and Reset

The chip has a built-in power-on reset circuit, so there is no need to connect a dedicated reset circuit externally.

The built-in power-on reset module will keep the chip in the reset state until the voltage is normal. When the voltage is lower than a certain threshold, the chip will also be reset.

When the external reset pin RST is low, the entire chip will be reset, and this pin can be left floating.



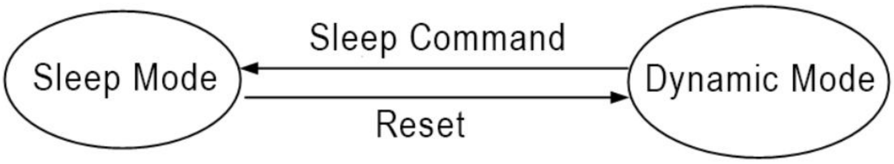
Power-on Sequence Diagram

External Reset Timing Diagram

Symbol	Description	Min	Max	Unit
Tpor	Chip initialization time after power-on	100	-	mS
Tpr	RST pin delayed pull-up time	5	-	mS
Tron	Chip reinitialization time after reset	100	-	mS
Trst	Reset pulse time	0.1	-	mS

Power-on and Reset Timing Description

7.2. Working Mode



Working Mode Conversion

- Dynamic Mode

  The IC is in this mode when there is frequent touch operation. In this mode, the touch chip quickly performs self-capacitance scanning, and reports touch info to the host. After there is no touch for 2 seconds, the IC will automatically enter standby mode (this function can be controlled by registers).

- Sleep Mode

  After receiving the sleep command, the IC enters sleep mode. In this mode, the touch chip is in a deep sleep state to save power consumption to the greatest extent and can be switched to dynamic mode through the reset pin.

7.3. Channel/Node Configuration

Each channel of CST816D self-capacitance touch chip supports self-capacitance scanning without external devices.

Supported self-capacitance size range for each channel: 1pF ~ 400pF.

7.4. I2C Communication

The chip supports the standard I2C communication protocol and can achieve a configurable communication rate between 10Khz~400Khz.

The two I2C pins, SCL and SDA, not only support open-drain mode, but also support internal pull-up mode for flexible selection.

7.5. Interrupt method

The touch chip will notify the host to read valid data through the IRQ pin only when a valid touch is detected and needs to be reported to the host, this can improve efficiency and reduce the burden on the CPU.

The interrupt edge can be configured to be valid on the rising edge or valid on the falling edge as required.

The IRQ pin is also used to wake up the host when a predefined gesture is matched in standby mode.

7.6. IIC Interface Description

The chip itself supports IIC operation, and the IIC pin can also be used for simple IO operation. Specific functions can be customized by the software according to specific projects.

a) IIC Address of The Device

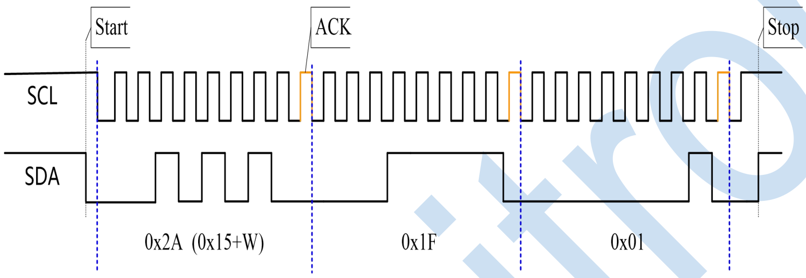
The 7-bit device address of the chip is generally 0x15, that is, the device write address is 0x2A, and the read address is 0x2B.

The iic address of some projects may be different, please consult the corresponding project and engineering personnel.

b) I2C Speed

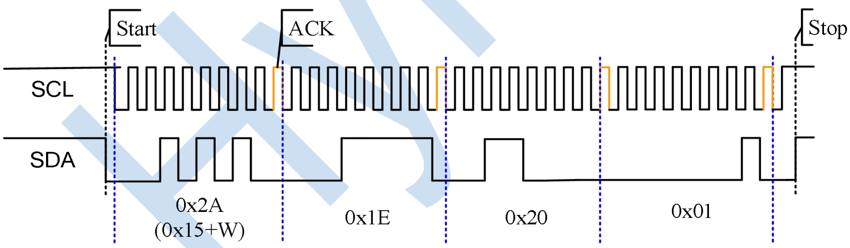
In order to ensure the reliability of communication, it is recommended to use a maximum communication rate of 400Kbps

c) Write A Single Byte



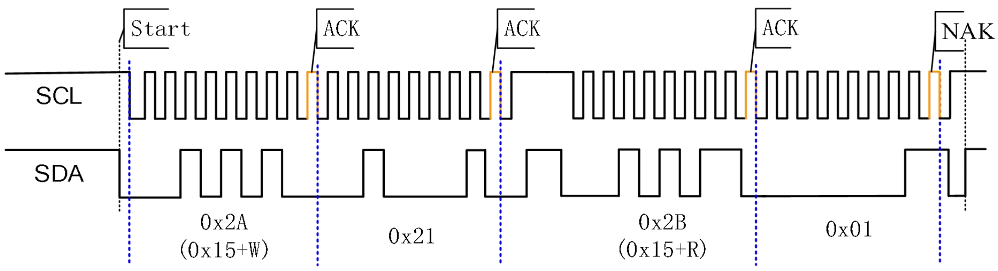
Write 0x01 to register 0x1F

d) Write Multiple Bytes Consecutively



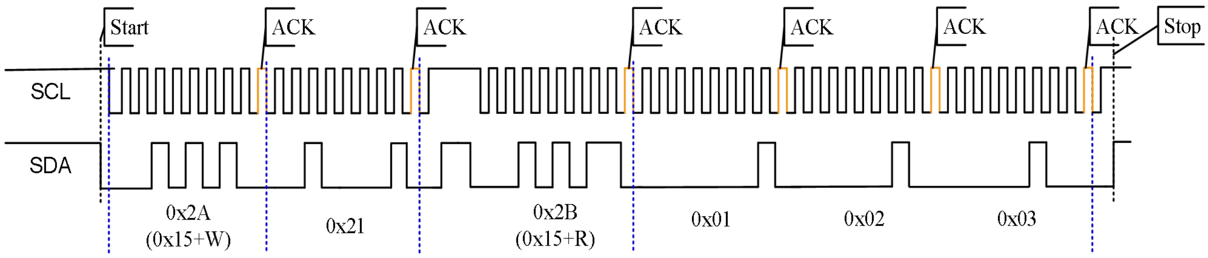
Write 0x20 and 0x01 to register 0x1E and 0x1F

e) Read A Single Byte



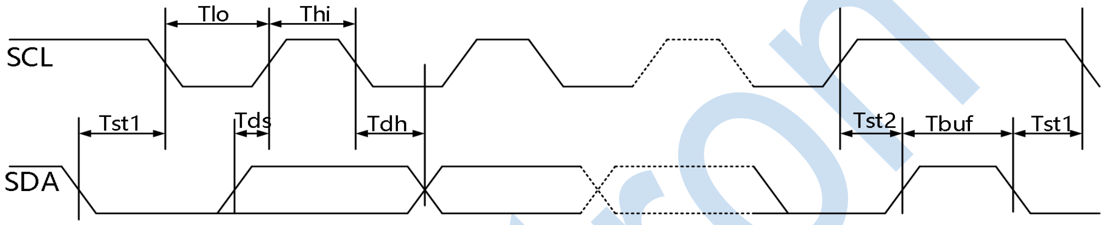
Read a single byte from register 0x21

f) Read Multiple Bytes Consecutively



Read 3 bytes from registers 0x21, 0x22, 0x23

g) Timing Description



Symbol	Description	Min	Typical	Max	Unit
Fscl	SCL clock frequency	10	-	400	kHz
Tst1	SCL hold time for START condition	0.6	-	-	us
Tlo	LOW period of SCL	1.3	-	-	us
Thi	HIGH period of SCL	0.6	-	-	us
Tds	SDA setup time	0.6	-	-	us
Tdh	SDA hold time	100	-	-	ns
Tst2	SCL setup time for STOP condition	0.6	-	-	us
Tbuf	Ready time between STOP and START	4.5	-	-	us

IIC Timing Description

8. Application Design Specifications

8.1. Power Supply Decoupling Capacitors

Generally, a 0.1uF and 10uF ceramic capacitors are connected in parallel at the VDD and VSS terminals of the chip to decouple and bypass.

The decoupling capacitor should be placed as close to the chip as possible to minimize the current loop area.

8.2. CMOD Filter Capacitor

The filter capacitor uses NPO/COG material capacitors with at least 10% accuracy, and the selection range of the capacitance value is between 1nF and 5.6nF, generally 1nF is selected. The specific optimum value is related to the corresponding body capacitance. The CMOD filter capacitor must be placed close to the corresponding pin of the chip, and the trace between the chip and the chip should be as short as possible.

8.3. Waterproof Precautions

There should be no large pieces of ground around the sensors and its traces. For large areas of ground, it must be broken.

8.4. ESD Considerations

The design of FPC will directly affect the effect of ESD. When designing, the following items must be paid attention to:

- ✧ It is recommended to use a magnetic film for full shielding for FPC and the magnetic film must be grounded.
- ✧ The lamination position of the FPC and the sensors should be as far away as possible from the gap of the assembled mechanism to reduce the impact of ESD.
- ✧ Consider adding a TVS tube to the ground at the power supply to enhance the anti-ESD interference performance.

8.5. Electromagnetic Interference Considerations

Sensor traces must be isolated from lines that may cause interference, such as power traces, audio lines, LCD drive lines, Bluetooth antennas, RF antennas, etc. When the TP adopts a full-fit design, it may be interfered by the LCD. In that case, the parameters of the TP need to be specially adjusted.

8.6. Ground

The high-precision detection circuit inside the touch chip is sensitive to the ground wire. If possible, the user should use a star ground to isolate the noise of other chips. At the same time, it is recommended to insert a magnetic bead at ground to enhance the anti-interference ability. If star grounding is difficult to achieve, the user should try to separate the ground of the high-current device from the ground of the touch chip.

9. Electrical Characteristics

Absolute Maximum Parameters

Symbol	Description	Min	Typical	Max	Unit
TSTG	Storage temperature	-40	25	125	℃
Ta	Operating ambient temperature when powered on	-20	-	85	℃
Vdd	Supply voltage relative to Vss	-0.3	-	+3.6	V
Vio	DC input voltage	VSS-0.3	-	VDD+0.3	V
LU	Latch-up current	-	200	-	mA
CDM	ESD Electrical Device Model	-	1000	-	V
HBM	ESD human model	-	8000	-	V

Absolute Maximum Parameters

AC Electrical Performance (Ambient temperature 25℃, VDDA=3.3V)

Symbol	Description	Min	Typical	Max	Unit
Fcpu	CPU frequency	-2%	20	+2%	MHz
F32k	Internal low-speed clock frequency	-5%	32	+5%	kHz
txRST	External reset pulse width	-	0.1	-	mS
tPOWERUP	Time from end of POR to CPU execution of code	-	4	-	mS
FGPIO	GPIO switching frequency	-	2	-	MHz
tRISE	Pin level rise time, Cload=50pF	-	32	-	nS
tFAIL	Pin level fall time, Cload=50pF	-	11.2	-	nS

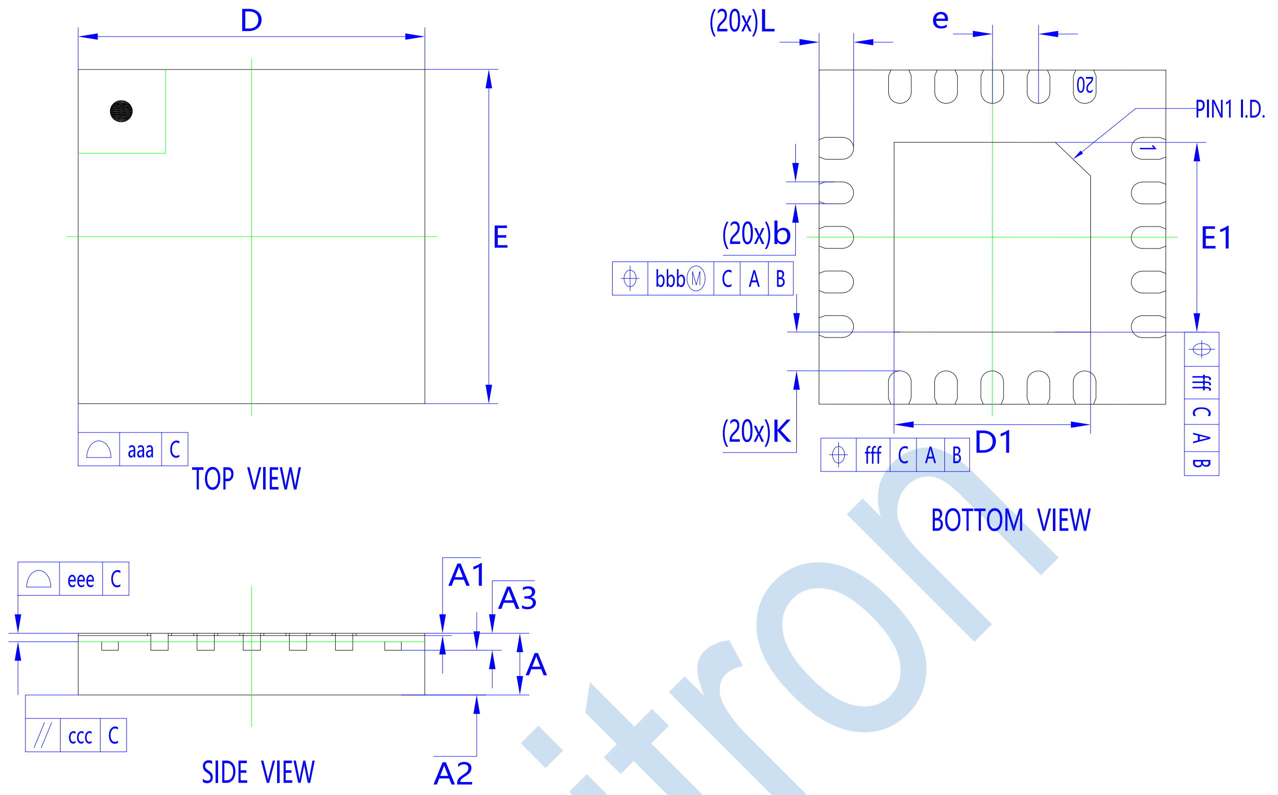
AC Electrical Characteristics

DC Electrical Performance (*Ambient temperature 25℃, VDDA=3.3V VIO = VDD/1.8*)

Symbol	Description	Min	Typical	Max	Unit
Vdd	Power supply	2.8	3.0	3.6	V
Rpu	Pull-up resistor	-	5	-	KΩ
Voh	High level output voltage	0.7* VIO	-	-	V
Vol	Low level output voltage	-	-	0.3* VIO	V
Ioh	High level output current	-	2.0	-	mA
Iol	Low level sink current	-	20.0	-	mA
Vil	Input low level voltage	-	-	0.3* VIO	V
Vih	Input high level voltage	0.7* VIO	-	-	V
Iil	Input leakage current	-	10	-	nA
Idd1	Operating current (dynamic mode)	-	1.8	-	mA
Idd3	Operating current (sleep mode)	-	2.0	-	uA
Vddp	Programming voltage	2.8	-	3.6	V

DC Electrical Performance

10. Product Packaging



Item		Symbol	Dimensions In Millimeters		
			Min	Nom	Max
Total Thickness		A	0.5	0.55	0.6
Stand Off		A1	0	0.02	0.05
Mold Thickness		A2	0.4		
L/F Thickness		A3	0.152		
Body Size	X	D	3		
	Y	E	3		
Exposed Pad Size	X	D1	1.6	1.7	1.8
	Y	E1	1.6	1.7	1.8
Lead Width		b	0.15	0.2	0.25
Lead Pitch		e	0.4		
Lead Length		L	0.2	0.3	0.4
Lead Tip To Exposed Pad Edge		K	0.2	--	0.35
Package Edge Tolerance		aaa	0.1		
Lead Offset		bbb	0.07	--	0.1
Mold Flatness		ccc	0.1		
Coplanarity		eee	0.08		
Exposed Pad Offset		fff	0.1		

11. Revision History

Version	Modification
V1.0	Initial release
V1.1	Revise seal information Update unified package POD parameters
V1.2	Unify action package name
V1.3	Update Operating current